AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 8, 12 and 15 without prejudice. Please add new claims 17-23.

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1. (CURRENTLY AMENDED) A circuit comprising:

a first pad circuit configured to transfer a first data signal in response to a pad control signal;

a second pad circuit configured to generate a second data signal from an input signal in response to said pad control signal;

a core logic configured to (i) exchange said first data signal with said first pad circuit, ~~and~~ (ii) receive said second data signal and (iii) generate ~~present~~ a control signal;

a first cell configured to (i) transfer said first data signal between said first pad circuit and said core logic and (ii) swap said first data signal and a test signal;

a second cell configured to (i) transfer said second data signal from said second pad circuit to said core logic and (ii) swap said second data signal and said test signal; and

a test circuit configured to (i) exchange said test data signal with said first cell and said second cell, (ii) store a test control signal, and (iii) multiplex said test control signal and said control signal to ~~present~~ generate said pad control signal.

2. (CURRENTLY AMENDED) The circuit according to claim 1, wherein (i) said test circuit ~~exchanges~~ transfers said test data signal ~~with~~ to said first cell ~~by presenting said test data signal to said cell,~~ and (ii) said first cell ~~swaps said data signal and said test data signal by overwriting~~ overwrites said first data signal with said test data signal~~, and (iii) said cell exchanges said data signal with~~ for transfer to said first pad circuit ~~by said pad circuit receiving said data signal from said cell~~.

3. (CURRENTLY AMENDED) The circuit according to claim 2, wherein said test circuit is further configured to clock said test data signal at a predetermined time to cause ~~said data signal received by~~ said first pad circuit to ~~change states~~ undergo a predetermined state transition for a transition response measurement of said first pad circuit.

4. (CURRENTLY AMENDED) The circuit according to claim 1, wherein (i) said second cell transfers said second data signal ~~exchanges said data signal between said pad circuit by pad circuit presenting said data signal~~ to said second cell~~,~~ and (ii) said second cell ~~swaps said data signal and said test data signal by overwriting~~ overwrites said test data signal with said second data signal~~, and (iii)~~ for transfer to said test circuit ~~exchanges said~~

~~test data signal with said cell by receiving said test data signal from said cell~~.

5. (CURRENTLY AMENDED) The circuit according to claim 4, wherein said test circuit is further configured to clock said test data signal to receive a sequence of samples for said second data signal ~~as received by said cell~~ as said input signal undergoes a predetermined state transition for a transition response measurement of said second pad circuit.

6. (CURRENTLY AMENDED) The circuit according to claim 1, wherein said test circuit comprises:

a multiplexer configured to multiplex said control signal and said test control signal to ~~present~~ generate said pad control signal; and

a controller configured to (i) store said test control signal, (ii) ~~present~~ transfer said test control signal to said multiplexer, and (iii) exchange said test data signal with said first cell and said second cell.

7. (ORIGINAL) The circuit according to claim 6, wherein said controller comprises:

an input configured to receive said test control signal; and

a user data register configured to (i) store said test control signal from said input and (ii) present said test control signal to said multiplexer.

8. (CANCELED)

9. (CURRENTLY AMENDED) A method of testing a pad circuit that transfers a data signal in response to a pad control signal, the method comprising the steps of:

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(A) generating a test control signal generated by a test circuit;

(B) multiplexing said test control signal and a control signal ~~presented~~ generated by a core logic co-located with said test circuit to generate said pad control signal ~~in response to step (A)~~;

(C) configuring ~~presenting said test control signal as said pad control signal to~~ said pad circuit with information from said test control signal ~~in response to step (B)~~; ~~and~~

(D) swapping said data signal of said pad circuit and a test data signal of a cell ~~in response to~~ after step (C); and

(E) measuring a response of said pad circuit based upon said test data signal.

10. (CURRENTLY AMENDED) The method according to claim 9, wherein step (D) comprises the sub-steps of:

transferring said test data signal to said cell ~~in response to step (C)~~;

first overwriting said data signal with said test data signal ~~in response to said transferring~~; and

first transferring ~~presenting~~ said data signal to said pad circuit in response to said first overwriting.

11. (CURRENTLY AMENDED) The method according to claim 10, wherein step (D) further ~~comprising the steps~~ comprises the sub-steps of:

clocking ~~the~~ said test data signal ~~in response to presenting~~ after said first transferring of said data signal to said pad circuit;

second overwriting said data signal with said test data signal ~~in response to clocking~~; and

second transferring ~~presenting~~ said data signal to said pad circuit in response to said second overwriting, wherein said response of said pad circuit comprises a transition response for driving an output signal.

12. (CANCELED)

13. (CURRENTLY AMENDED) The method according to claim ~~1~~ 9, wherein step (D) comprises the sub-steps of:

first receiving said data signal at said cell ~~in response to step (C)~~;

first overwriting said test data signal with said data signal ~~in response to said receiving said data signal~~; and

first transferring said test data signal from said cell ~~in response to said overwriting~~ to said test circuit.

14. (CURRENTLY AMENDED) The method according to claim 13, wherein step (D) further ~~comprising the steps~~ comprises the sub-steps of:

second receiving said data signal ~~in response to transferring said test data signal~~;

second overwriting said test data signal with said data signal ~~in response to said second receiving~~; and

second transferring said test data signal from said cell ~~in response to said second overwriting~~ to said test circuit, wherein said response of said pad circuit comprises a transition response to an input signal.

15. (CANCELED)

16. (CURRENTLY AMENDED) A circuit comprising:

~~first~~ means for transferring a data signal, ~~in response to~~ said means for transferring being configured by a first control signal;

~~means for exchanging said data signal with said first means for transferring;~~

means for ~~presenting~~ generating a second control signal;

~~second means for transferring said data signal between said first means for transferring and said means for exchanging;~~

means for swapping said data signal and a test signal;

~~means for exchanging said test data signal with said second means for transferring;~~

~~means for storing~~ generating a third control signal; ~~and~~

means for multiplexing said third control signal and said second control signal to ~~present~~ generate said first control signal; and

means for measuring a response of said means for transferring based upon said test data signal.

17. (NEW) The circuit according to claim 1, wherein said pad control signal comprises an enable signal configured to alternatively enable and disable an output drive capability of said first pad circuit.

18. (NEW) The circuit according to claim 1, wherein said pad control signal comprises a receive enable signal configured to alternatively enable and disable a receive capability of said first pad circuit.

19. (NEW) The circuit according to claim 1, wherein said pad control signal comprises a signal configured to alternatively enable and disable an active termination of said second pad circuit.

20. (NEW) The circuit according to claim 1,wherein said pad control signal comprises a signal configured to control a noise margin threshold of said second pad circuit for said input signal.

21. (NEW) The circuit according to claim 1, wherein said control signal comprises a plurality of signals and said multiplexer comprises a plurality of multiplexers, one for each of said signals.

22. (NEW) The circuit according to claim 21, wherein at least one of said first pad circuit and said second pad circuit receives a subset of said signals.

23. (NEW) The circuit according to claim 16, wherein a1 said response for said means for transferring is a transition response between a high state and a low state.